Many a time designers find themselves in pretty confusing start when it comes to simulating multilayer VIA structures for High Speed or High Frequency Applications? As we all understand performing EM simulations are the best way to characterize VIA structures however confusion creeps in if designers think in terms of which EM simulation technology is the best suited and the selection has to be done between Planar EM solvers i.e. solvers based on Method of Moments (MoM) or using Full 3D solvers based on FEM or FDTD techniques.

This paper is an effort to present a comparative study between these solvers as available under Agilent ADS software so that designers can make best use of the simulations technologies as suited for their applications.

**Multilayer VIA drawing wizard:**

Drawing multilayer via geometries is made pretty easy using Multilayer VIA wizard introduced in ADS2012 release. To activate VIA drawing utility, select **ADS Main Window->Tools->Manage AEL AddOns** and select **VIA Drawing Utility**.

Click Close button and restart ADS.

Once ADS is restarted, created a new ADS workspace with the desired name and select “mil” as the drawing unit using the new workspace creation wizard.
Case Study: 5-layer VIA

Before we use VIA drawing utility we need to have our stackup and layer definitions ready. In this tutorial we shall create our own layers so that designers are educated on how to add our own layer definitions as well as create a new multilayer dielectric definition from scratch.

1. We shall start our case study by defining our own 5 metal layers and 4 VIA layers.
2. From ADS Main Window, select Options->Technology->Technology Setup, select Show Other Technology Tabs and window shown as next snapshot will appear. Go to Layers Tab

3. Click on Add Layer to see a new layer with some default name getting added, repeat this to add total of 9 layers (5 metal layers and 4 VIA layers). Once done rename these layers as metal1, metal2, metal3, metal4, metal5, via1, via2, via3, via4. For metal1-5 define process role as Conductor (which is default) and for via1-4 define the process role as Conductor VIA as shown below

Process role doesn’t affect our simulation results in any manner but it helps us to organize layers in database properly and we shall see the effect of that while creating the substrate where we have to do little less work.

Once done, click OK. Now we have all the layers to start preparing our substrate stackup for VIA creation and simulation.
4. Open a layout cell by clicking on Layout icon in the Main ADS window or by selecting File->New->Layout from the main ADS window.

5. Click on Substrate icon present in the EM toolbar of the layout window and select OK in the pop window which 1st intimates us that there is no substrate present and then we select default substrate as a template for our own substrate stackup creation. Once done a default microstrip substrate would be available as shown below.

6. Right click on Alumina substrate and select option “Insert Substrate Layer Above”, repeat it to add 5 dielectric layers as shown below.

7. Right click on the bottom cover and select “Delete Cover” to remove the infinite ground plane from the bottom. Left click on lowest Alumina and select the material to be “AIR”.

8. Click on the substrate interface above metal1 and select the Interface to be “SLOT Plane”. (SLOT is a negative ground plane in ADS). Repeat the same for 2 more interfaces.

9. Right click on interface above metal1 and select “Map SLOT Layer” and notice that metal2 is mapped to this interface. Repeat the same at 2 interfaces above to see metal3 and metal4 getting mapped.

10. Right click on the topmost interface and select “Map Conductor Layer” and see metal5 will be mapped as conductor making it TOP conductor as shown in the next snapshot.
11. Now we have conductors on top and bottom layer and need to define the VIA mapping between these conductors. We can either create a stacked VIA or a thru VIA definition, for simulation results it really doesn’t matter and layout designers make it based on their convenience. In this case study we shall use stacked VIA definition and for that we need to have a separate VIA layer on each dielectric.

12. Right click on the substrate between metal5 and metal4 and select “Map Conductor VIA” and notice that “via1” layer is mapped as VIA between metal5 and metal4 layer. Repeat it for all the substrate layers to see via2, via3 and via4 getting mapped as shown below.

It is good time to recall that we define process role for these layers and they were having layer numbers assigned when we created them and it helps ADS to assign these layers during substrate creation in increasing layer number order and keep track if we are mapping conductors or VIAs. Even if we do not define a process role we can always change the layer name once the object (i.e. conductor or via) is mapped to dielectric stackup but that would require little manual work.
13. Now we have the stackup definition ready, remaining thing is to specify the material properties and thickness etc. Click on each substrate stackup layer shown as Alumina and define the thickness as 5 mils.

14. Click on Technology->Material Definitions and in the Dielectric Tab, click on Add from Database and select FR4 from the list and click OK.

15. Go to Conductor tab and select Copper from available conductors list and click OK

16. Click OK on the material definition window and select each dielectric layer and change the material to FR4 as shown below

17. Click on metal1 and select material as Copper, thickness as 35um, Operation as “Intrude into substrate” and position as “Below Interface” so that this metal is defined as thickness of 35um which is growing on the lower side of the stackup.

18. Click on metal5 and select material as Copper, thickness as 35um, Operation as “Intrude into substrate” and position as “Above interface” as we want it to grow upwards.

19. Once done dielectric stackup will appear as shown below.
Using Multilayer VIA utility in ADS:

1. From the layout window, select Add-Ons->Via Drawing Utility
2. In the pop-up window of via drawing utility select 5 layers
3. Select metal5 downwards to metal1 against each conductor (as per our stackup definition)
4. Select via1 to via4 against each dielectric layer.
5. Define metal1 and metal5 type as Signal and rest as Slot Plane as shown below

6. In the Board Outline define board outline dimension of Width=400 and Length=600 and select layer as ads_supply (this is only to draw the board outline)
7. Define all Hole diameters as 16 with Signal Pad on metal1 and 5 layer = 24, Antipad dimensions for SLOT layer as 40
8. Define VIA type as Differential with Spacing as 50 and select Ground VIA as Center to draw a ground VIA between the Differential VIAs
9. Under Connecting Traces, define the parameters as shown here:
10. Once done, it will appear as below

![Board Outline with different layers and trace settings](image1)

11. Click on Draw to see differential VIA geometry drawn in ADS layout as shown below

![Differential VIA geometry](image2)
12. Click on EM Setup icon in the EM Toolbar

Click on 3D View icon to inspect geometry in isometric fashion as shown below:
a. Select on Mom uW and select Simulator as Momentum RF (this is quasi static mode which is ideally suited for electrically small structures as VIAs). Momentum Microwave can also be selected but RF mode would be faster and produces quite accurate results for geometries which are less than half-wavelengths.

b. Click on Substrate and make sure we are using our 5 layer stackup definition

c. Click on Ports to ensure there are 4 Ports connecting between P1-4 to Gnd. GND here is reference to the SLOT planes which are negative ground reference planes.

d. Click on Frequency Plan and define the frequency sweep from 0-10 GHz with 50 (max) points and Adaptive Sweep.

e. Click on Options and go to Mesh Tab and enter Cells/Wavelength = 50 to ensure enough cells for accurate computation. For larger geometries default value of 20 is quite sufficient, however for smaller geometries such as present case we need to change it to little higher number such as 50 or 100 for little denser mesh.

f. Click on Simulate icon to start the EM simulation and it will take couple of minutes to compute Substrate’s Green Functions (one time) and simulation will finish in less than a minute.

13. Once the simulation is finished, data display window as shown here would be available with the simulation results

14. Close the data display window and go to EM setup window again and change the Simulator to FEM.

15. Click on Options->Mesh->Stop Criterium as 0.02 (delta error in S-matrix for mesh to converge) as shown in next snapshot.
16. Click on Simulate button and see that FEM simulator is invoked to simulate the VIA structure and now it takes some time to simulate the structure and it is not as fast as Momentum RF simulator.

17. Once FEM simulation is finished a new data display will be opened with FEM simulation results.

18. Once we plot Momentum and FEM simulation results on these graphs, below is the comparison:

Here, Red traces are FEM simulation results and Blue indicates Momentum simulation results and it can be seen that Momentum and FEM simulation results are pretty close and we can use Agilent Momentum for accurate multilayer VIA simulations as it is lot faster in simulating multi-layer VIA structures as compared to FEM.
Case Study: 10-layer VIA

Using the same process, we added 5 more metal layers and 4 VIA layers in the Layers window and modified the stackup for 10 layers as shown below.

3D View of 10-layer VIA (ground planes hidden for better visibility)
Result Comparison:

Pretty much like earlier simulation, Momentum RF and FEM simulations were performed and below are the results comparisons:

Here, Red traces are FEM simulation results and Blue indicates Momentum simulation results and it can be seen that Momentum and FEM simulation results are pretty close but Momentum is lot faster in simulating multi-layer VIA structures.

Conclusion:

Momentum simulator based on Method of Moments technology in ADS 2012 has come of age and it is pretty accurate simulator to perform simulation on High Speed applications and to simulate multi-layer VIA structures with confidence as shown in this tutorial. While providing great accuracy it takes much lesser time as compared to FEM and other technologies so that designers can optimize and fine tune their VIA interconnects faster with greater confidence.

Having said that, FEM simulator is also available as tightly integrated module within ADS environment for designers to make use of full 3D simulator technology whenever required and these results can be integrated for overall Channel analysis for High Speed Digital Application.

Resources:

1. Agilent EEsof Website: [www.agilent.com/find/eesof-ads](http://www.agilent.com/find/eesof-ads)
3. Agilent EEsof on YouTube: [www.youtube.com/AgilentEEsof](http://www.youtube.com/AgilentEEsof)
6. Applications You Tube: [www.youtube.com/user/BhargavaAnurag](http://www.youtube.com/user/BhargavaAnurag)
7. Anurag Bhargava: [anurag_bhargava@agilent.com](mailto:anurag_bhargava@agilent.com)